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<u>L33</u>	19 and 114	0	<u>L33</u>
<u>L32</u>	19 and 113	1	<u>L32</u>
<u>L31</u>	112 and 118	1	<u>L31</u>
<u>L30</u>	112 and 117	1	<u>L30</u>
<u>L29</u>	112 and 116	0	<u>L29</u>
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<u>L27</u>	112 and 114	6	<u>L27</u>
<u>L26</u>	112 and 113	5	<u>L26</u>

<u>L25</u>	l11 and l18	6	<u>L25</u>
<u>L24</u>	l11 and l17	6	<u>L24</u>
<u>L23</u>	l11 and l16	0	<u>L23</u>
<u>L22</u>	l11 and l15	12	<u>L22</u>
<u>L21</u>	l11 and l14	12	<u>L21</u>
<u>L20</u>	l11 and l13	31	<u>L20</u>
<u>L19</u>	l12 and "OR" and "AND"	83	<u>L19</u>
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<u>L18</u>	(716/18)[CCLS]	1024	<u>L18</u>
<u>L17</u>	(716/18)![CCLS]	1024	<u>L17</u>
<u>L16</u>	(326/41,114,125)![CCLS]	1562	<u>L16</u>
<u>L15</u>	(712/2-300)[CCLS]	12144	<u>L15</u>
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<u>L13</u>	(716/2-19)![CCLS]	9098	<u>L13</u>
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<u>L12</u>	L11 and (overal\$4 or composit\$3 or final or roll\$5 or accumulat\$6 or sum\$7) near5 result\$1	113	<u>L12</u>
<u>L11</u>	l7 and disjunct\$4	364	<u>L11</u>
<u>L10</u>	L9 and (rol\$5 or composit\$3 or sum\$7)	1	<u>L10</u>
<u>L9</u>	5682519.pn. and (cmos or static\$6)	1	<u>L9</u>
<u>L8</u>	5682519.pn. and static\$6	0	<u>L8</u>
<u>L7</u>	boolean and short\$3 and conjunct\$4	8055	<u>L7</u>
<u>L6</u>	L4 not l2	4	<u>L6</u>
<u>L5</u>	L4not l2	35	<u>L5</u>
<u>L4</u>	boolean near12 (gate\$1 or circuit\$4 or path\$1) near15 static	39	<u>L4</u>
<u>L3</u>	L2 not l1	6	<u>L3</u>
<u>L2</u>	boolean near8 (gate\$1 or circuit\$4 or path\$1) near12 static	35	<u>L2</u>
<u>L1</u>	boolean near5 (gate\$1 or circuit\$4 or path\$1) near10 static	29	<u>L1</u>

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IEEE JNL	IEEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
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



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